Fraunhofer IIS

ADC16b010kS350nm

16 Bit 10 kS/s Incremental Delta-Sigma ADC

Key Parameters

- Resolution: 16 bit
- Conversion rate: up to 20 kS/s
- Power consumption: 13 mW @ 2.5 V
- Integral non-linearity: +/- 3 LSB
- Diff. non-linearity: +/- 0.7 LSB
- Supply voltage: 2.4 V – 3.6 V
- Operation clock: 1.0 – 5.5 MHz
- Differential input: +/- 1.0 V

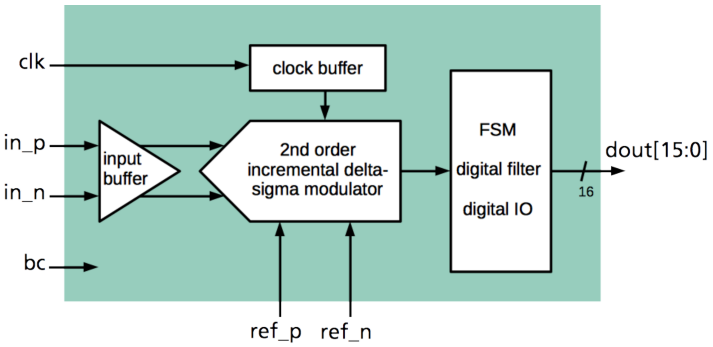

Fig. 1: IP-Level Block Diagram

General Description

On the one hand, incremental delta-sigma modulators are able to **convert DC and multiplexed input signals** as known from Nyquist ADCs. On the other hand, using internal oversampling and noise shaping provides **high linearity** as known from delta-sigma ADCs.

This **fully differential** ADC is designed to convert full swing (-1V to +1 V) input signals as well as unipolar input signals (0 V to +1 V), each with 16 bits resolution. Low-frequency **noise reduction** is provided using chopper-modulation.

The **embedded power down mode** provides a linear relation between power consumption and conversion rate of the ADC. Scaling between power consumption, conversion rate and resolution can be achieved due to the selectable number of conversion cycles.

The analog ADC frontend can also be used in combination with a custom digital filter for classical delta-sigma operation.

The ADC is **silicon evaluated** using the **AMS H35** process. Measurement results and samples are available.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

Benefits

- Low design risk due to silicon evaluated design
- Easy to use input due to integrated input buffer
- Selectable power consumption due to integrated automatic power-down function
- Task dependent selectable resolution
- Flexible use due to single-conversion and continous-conversion mode

Deliverables

- GDSII data
- Simulation model
- Documentation
- Silicon validation report
- Integration support

FACT SHEET

CONTACT

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